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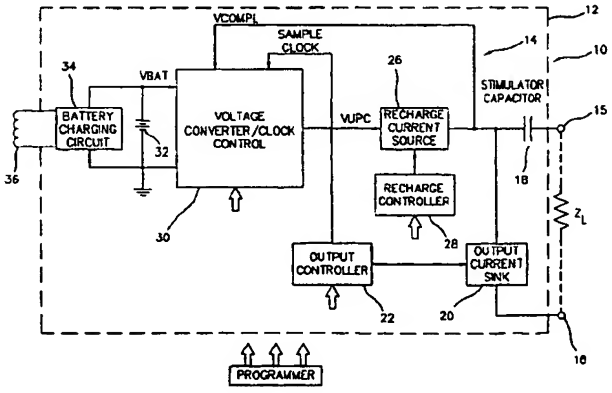
(54) Title: VOLTAGE CONTROL CIRCUITRY FOR CHARGING OUTPUT CAPACITOR



(57) Abstract: Voltage control circuitry (30) driven by a battery (32) for producing a supply for charging an output capacitor (18), which is periodically discharged to supply a current pulse to an impedance load (Z_L), e.g., body tissue. The voltage control circuitry (30) converts the battery voltage VBAT to a charging voltage VUPC based upon programmed parameters and the value of the voltage VCOMPL measured at one terminal (15) output capacitor. The circuitry includes a voltage converter (30) for multiplying VBAT by a multiplication factor to produce VUPC. The voltage VCOMPL is sampled to determine its final "droop" at the end of an output current pulse. If the final droop value is lower than a certain threshold, then the voltage converter switches to increase the charging voltage VUPC. If the final droop value is above a certain threshold, then the voltage converter switches to reduce the value of the voltage VUPC. This feedback action maintains the output voltage within an acceptable operating range to provide sufficient energy to produce an efficacious output current pulse for stimulation without causing unproductive energy loss, e.g., heat. In order to avoid premature depletion of battery energy, the charging voltage VUPC is compared with the output voltage VCOMPL to determine the optimum clock rate to be used to convert VBAT to VUPC.

WO 01/08282 A1

TITLE: VOLTAGE CONTROL CIRCUITRY FOR CHARGING OUTPUT CAPACITOR

FIELD OF THE INVENTION

This invention relates generally to voltage control circuitry suitable for charging an output capacitor used to periodically supply an output current pulse. The invention is particularly suited for use in a battery powered device intended to be implanted in a patient's body for supplying a current pulse to stimulate body tissue.

BACKGROUND OF THE INVENTION

Implantable devices for stimulating body tissue are known in the prior art. For example, see U.S. Patent 5193539 by Schulman, et al, assigned to the same assignee as the present application. Such devices typically store energy in an output (or "stimulation") capacitor which is periodically discharged to supply an output current pulse to stimulate targeted tissue. The energy source primarily discussed in the 5193539 patent for charging the capacitor is comprised of an external source for generating an alternating magnetic field. The alternating field energy is inductively coupled to an internal power supply circuit for producing a voltage for charging the stimulation capacitor. Unfortunately, such prior art devices require that a patient remain in very close proximity to the external source to enable the devices to continue to operate. For example, such devices are typically limited to operating for only several seconds to a minute or so without requiring additional energy from the external source.

More recent implantable devices have incorporated rechargeable batteries capable of operating for prolonged periods, in excess of one hour and up to many days, without requiring additional energy from an external power source. This difference in independent operating duration

leads to a qualitative difference in the utility of the device and how effectively the devices can serve a patient.

In such battery operated implantable devices, it is very desirable to control the energy transfer from the battery to the output capacitor in a manner to minimize energy inefficiencies, i.e., unproductive energy losses, while also retaining the ability to control the amplitude, duration, and frequency of output current pulses supplied by the output capacitor to an impedance load, e.g., body tissue.

SUMMARY OF THE INVENTION

The present invention is directed to voltage control circuitry driven by a battery for producing a voltage for charging an output capacitor. The voltage control circuitry converts the battery voltage VBAT to a charging voltage VUPC based upon programmed parameters and the value of the output voltage VCOMPL measured at one terminal of the capacitor.

In many tissue stimulation applications, it may be medically efficacious to produce a high amplitude current across a high magnitude tissue impedance between output electrodes. This situation necessitates the application of a high amplitude charging voltage VUPC to the output capacitor. In accordance with the preferred embodiment, the voltage control circuitry includes an up/down voltage converter for deriving the charging voltage VUPC based on the battery voltage VBAT. The conversion can be implemented by known techniques including, for example, placing a plurality of converter capacitors in parallel across a voltage source for charging, and then switching the capacitors into a series configuration to produce a voltage equal to some multiple of the source voltage. Alternatively, the converter capacitors can first be placed in series across the voltage source and then switched to a parallel configuration to produce a voltage equal to some fractional value of the source voltage.

In accordance with the preferred embodiment, the output capacitor voltage is sampled at a specific point in time relative to each discharged current output pulse to generate the signal VCOMPL.

In accordance with a significant feature of the preferred embodiment, the charging voltage VUPC is compared with the output capacitor voltage VCOMPL to determine a clock rate used to convert VBAT to VUPC. For example, the clock rate can be off, slow, or fast depending upon the charge condition of the output capacitor. This feature is useful to conserve energy and avoid premature depletion of battery energy.

More particularly, in accordance with the preferred embodiment, the output voltage, sometimes referred to as the "compliance" voltage VCOMPL, is sampled to determine its final "droop" at the end of an output current pulse. If the final droop value is lower than a certain threshold (ΔV_{LOWER}), then the voltage converter switches to increase the converter charging voltage VUPC. On the other hand, if the final droop value is above a certain threshold (ΔV_{UPPER}), then the voltage converter switches to reduce the value of the voltage VUPC. This feedback action maintains the output capacitor voltage within an acceptable operating range to provide sufficient energy to produce an efficacious output current pulse for stimulation without causing unproductive energy loss, e.g., heat.

Exemplary embodiments of the invention intended for tissue stimulation are configured to be accommodated in a small implantable housing preferably having an axial dimension of less than 60 mm and a lateral dimension of less than 6 mm so as to be readily injectable. Devices in accordance with the invention preferably operate from a 2.4 to 4.5 V battery to provide stimulation output current pulses having a controllable amplitude of between 5 microamps and 20 milliamps, a controllable pulse width of between 10 microseconds and 2 milliseconds, a controllable repetition rate of between 1 pulses per second (pps) and 1000 pps.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other features and advantages of the invention will be more apparent from the following detailed description wherein:

Figure 1a shows a block diagram of voltage control circuitry in accordance with the present invention;

Figure 1b shows an output current pulse produced by discharging an output capacitor, the output capacitor voltage, and a sample clock;

Figure 1c shows a block diagram of the voltage converter/ clock control circuit of Figure 1a;

Figure 1d shows the diagram illustrating field effect transistor (FET) drain current (I_D) versus drain-source voltages (V_{DS}), for different gate source voltages (V_{GS});

Figure 2a indicates the automatic compliance voltage adjustment circuitry in block diagram form;

Figure 2b shows the compliance test in block diagram form;

Figure 2c indicates the pump clocking control in block diagram form;

Figure 3a shows the voltage converter and output circuitry;

Figure 3b shows the current mirror-based circuit for producing a sub-threshold reference voltage;

Figure 4 depicts the ideal switch model for the up/down converter;

Figure 5 shows the different up/down converter states for each of the scale factors, the Figure 5 has seven parts, Figures 5a through 5g;

Figure 5a shows the switch and capacitor settings in a charging configuration (S0) and in a discharging configuration (S1) for a multiplying factor of ½, i.e., a down-conversion mode;

Figure 5b has an analogous depiction for a multiplication factor of 1;

Figure 5c pictures an analogous situation for a multiplication factor of 1.5;

Figure 5d shows an arrangement for the multiplication factor of 2;

Figure 5e presents the switch and capacitor combinations for the multiplication factor of 2.5;

Figure 5f shows the similar situation for the multiplication factor 3;

Figure 5g is an analogous presentation for the multiplication factor 4.

DETAILED DESCRIPTION

Attention is initially directed to Figure 1a which is a block diagram of a preferred implantable device 10 including a housing 12. The housing contains electronic circuitry 14 for producing a current pulse between output electrodes 15, 16 through a load impedance Z_L, e.g., body tissue. The electronic circuitry 14 includes an output (or "stimulator") capacitor 18 and an output current control device, e.g. current sink 20. The current sink 20 is controlled by an output controller 22. By activating current sink 20, capacitor 18 can discharge through sink 20 to produce an output current pulse through load impedance Z_L. The characteristics of the current pulse, e.g., amplitude, duration, repetition rate, are defined by controller 22 which is preferably programmable by an external programmer 24. The programmer 24 communicates with controller 22 via a communication channel, e.g., radio frequency (RF), not shown.

A recharge current control device, e.g. current source 26 is also connected to capacitor 18 to selectively apply a charging current to the capacitor. Current source 26 is controlled by recharge controller 28. Controller 28 is preferably programmable by external programmer 24 to

control, for example, the on/off timing of current source 26. When source 26 is on and sink 20 is off, a current is applied to capacitor 18 to charge the capacitor toward voltage VUPC.

The voltage VUPC is produced in accordance with the present invention by a voltage controller / clock control circuit 30. The circuit 30 produces the voltage VUPC as a function of an applied battery voltage VBAT supplied by battery 32. Battery 32 is preferably rechargeable via a charging circuit 34. Energy is preferably supplied to the charging circuit 34 via coil 36 from an external source (not shown) generating an alternating magnetic field.

The circuit 30 is preferably programmable by external programmer 24. The circuit 30 functions to define a multiplication factor which relates VUPC to VBAT. That is, circuit 30 acts as an up/down voltage converter to multiply VBAT by a factor to produce VUPC. The factor can preferably be an integer or fraction and is determined based on the voltage value VCOMPL derived from capacitor 18.

Attention is now directed to Figure 1b which in line (a) represents an output current pulse 40 which is discharged by capacitor 18 through load Z_L. The wave form shows the current at a zero level between times t1 and t2. Line (b) represents the voltage VCOMPL at the positive terminal of capacitor 18 and is shown to be at level VUPC between times t1 and t2. Now assume that output current sink 20 turns on at time t2 to increase the output current pulse amplitude to A1 which is maintained to time t5, as dictated by controller 22 controlling output current sink 20.

Figure 1b line (b) shows how the voltage VCOMPL varies between times t2 and t5 as capacitor 18 discharges through load Z_L. Between times t3 and t4, controller 22 generates a sample clock 42 to measure VCOMPL to determine the value of its final "droop" 44, i.e., the value reached by VCOMPL proximate to the end of the output current pulse at time t5. This measured value of VCOMPL at the sample clock is used by the voltage converter / clock control circuit 30 of Figure 1a to select a multiplication factor to produce VUPC from VBAT.

Note that line (b) of Figure 1b represents a low threshold 46 (ΔV_{LOWER}) and a high threshold 48 (ΔV_{HIGHER}) against which the droop value 44 will be compared to determine whether the multiplication factor, defined by circuit 30, should be adjusted. Also note that line (b) of Figure 1b represents a difference 49 between the target charging voltage VUPC and the value of VCOMPL at t6 after the capacitor 18 has been recharged via current source 26. As will be discussed hereinafter, the magnitude of the difference 49 is used to control a clock rate which determines the rate at which the multiplication factor can be adjusted.

Attention is now directed to Figure 1c which shows a block diagram of the voltage converter / clock control circuit 30 of Figure 1a. The circuit 30 includes a compliance test circuit 50, a converter switch control circuit 52, a converter switch bank 54, a clock controller circuit 56 and a comparator 58. The circuits 50, 52 and 54 function to convert the voltage VBAT to produce the charging voltage VUPC. Briefly, the compliance test circuit 50 examines the relationship between the capacitor droop voltage 44 (i.e., VCOMPL at the sample clock) and the aforementioned thresholds 46, 48 to determine whether multiplication factor should be increased or decreased. The switch control circuit 52 then generates a command, supplied to switch bank 54 via lines 60, to operate individual switches in bank 54 to implement the desired multiplication factor.

The circuits 56, 58 function to respond to the difference value 49 (Figure 1b line (b)) to establish an optimum clock rate for switch control circuit 52. That is, although it is desirable to reduce the difference value 49 to zero, excessive adjustment of the multiplication factor is wasteful of limited energy resources available from battery 32. The clock controller 56 functions to produce a clock rate on line 61 which is optimized to conserve energy and yet maintain the charged voltage on capacitor 18 at close to VUPC.

It is pointed out that the output current sink 20 and recharge current source 26 of Figure 1a are preferably fast acting, low loss circuits. In a preferred embodiment of the invention these circuits are implemented as

field effect transistors (FET). Figure 1d depicts the constant current characteristic of a typical FET wherein the drain current ID is essentially flat over a wide drain-source voltage (V_{DS}) range. The drain current amplitude is primarily a function of the gate-source voltage V_{GS}. In Figure 1a, the voltage V_{GS} for current sink 20 is controlled by controller 22 and the voltage V_{GS} for current source 26 is controlled by controller 28.

Attention is now directed to Figure 2a which depicts an exemplary implementation of the conversion portion of Figure 1c comprising the compliance test circuit 50, the switch control circuit 52 and the converter switch bank 54. The switch bank can use a well-known method for up-conversion by placing capacitors in parallel across a voltage source for charging so that each capacitor is charged to that voltage. Then the capacitors are placed in a series configuration (by switching means) such that the overall voltage is the sum of the voltages on the individual capacitors. A similar method, old in the art, of placing, say, two same value capacitors in series and charging the group in parallel with the voltage source, will give one half of the voltage source voltage when those two same value capacitors are used in parallel without the battery. Bank 54 is depicted in Figure 2a as having multiple switch inputs SW1-SW14 for controlling multiple FET switches internal to bank 54. These internal switches control multiple capacitors, e.g., C1-C3, to achieve the desired multiplication factor.

The compliance test block diagram is shown in Figure 2b, while Figure 2c illustrates the pump control block diagram. The goal of the compliance test block is to determine when the compliance voltage VCOMPL is too high or too low. The switch control circuit clocking controls the switching rate of the FET switch bank 54. The switching rate is reduced to the extent possible to reduce power consumption. In Figure 2b, the compliance voltage VCOMPL is compared to either [VBAT + 1] volt or [0.7 VBAT] volt, and the GO_UP (201) or GO_DOWN (202) decision outputs direct the switch control block (52) to take action.

This upconverter takes the battery voltage VBAT (Figure 3a, 100) and multiplies it by a programmed scale factor, set by lines SCALE_0 (301), SCALE_1 (302), and SCALE_2 (303), to generate the voltage, VUPC (304), necessary for a pulse generation circuitry. The multiplication factors in the version of the up/down converter shown are ½x, 1x, 1½x, 2x, 2½x, 3x, and 4x. A different set or an expanded set of multiplication factors can be implemented with more capacitors and switches, as desired.

The control bits are loaded into an up/down counter using the LOADN (305) line. A low on the reset line, RESETN (306), places the converter in the 1x scale factor setting.

The upconverter can be placed in automatic adjustment mode so that the scale factor moves to the optimal value based on sampling of the compliance voltage, VCOMPL (307), measured at the end of the stimulation pulse.

The time at which to sample the compliance voltage is controlled with the SAMPLE_CLK (308) line. At that time, the automatic adjustment of the battery voltage multiplier circuit is based on the amount of "unused" compliance voltage left at the end of the stimulation pulse. If the "unused" compliance voltage is below a hardwired threshold, Vlower, where Vlower is typically is the range 0.1 V to 0.8 V, then this indicates, or is defined as the case that, there was insufficient voltage to adequately drive the desired pulse amplitude. The multiplier factor will increase to the next higher multiple.

If the "unused" compliance voltage is above an upper hardwired threshold, Vhigher, this indicates that there is excess compliance voltage, and the factor will decrease to the next lower multiple as a power-saving feature. Vhigher is set to either [0.7 VBAT] or [VBAT + 1v] depending on the currently set scale factor.

Voltage conversion is achieved by switching among the input voltage and up to three capacitors, and depositing charge on a fourth, or

reservoir, capacitor. Clocking within the switched-capacitor section occurs at a normal frequency of 20 kHz.

When sufficient charge to reach the target voltage has been deposited on the stimulation capacitor, CSTIM (309), the clock can be automatically set to a lower rate (which could be 0 Hz) to save power. This shutdown point is determined by monitoring the compliance voltage, VCOMPL (307), and comparing it to the upconverter output voltage minus a hardwired threshold [VUPC -0.1V] (Figure 2c, 204). The automatic scaling and clock shutdown modes are set with the MODE_0 (310), MODE_1 (311) or MODE_2 (312) lines.

Power can be saved by automatically decreasing upconverter clock rate to a lower frequency. The switching of the FET switches in the switch bank 54 consumes power proportional to the rate of switching. The automatic adjustment of the voltage converter clock rate is based on the state of charge of the stimulation capacitor 18. After a stimulation pulse has drained charge from the stimulation capacitor, recharge current is supplied to it and the voltage on it will rise toward the upconverter voltage. As the voltage on the stimulation reservoir capacitor nears the voltage VUPC, it passes a threshold, which triggers the switching of the upconverter rate to a lower frequency, which includes a frequency of zero Hz.

A control signal is generated and used to lower the multiplier factor of the upconverter. A comparator is used to compare a reference voltage with the compliance voltage at a particular sample time, viz., the end of the stimulation pulse. As another power saving feature, the reference voltage and the comparator are only powered during this sample time interval. A capacitor normally in parallel with the battery is stacked on top of the battery during the sampling interval. This is a voltage doubler.

This voltage is used to power the comparator and is also used to turn on a diode-connected FET that feeds into the positive side of the battery. The FET -diode circuit part provides a voltage drop across the diode, due to the small but finite conducting resistance of the diode. This one diode

voltage drop provides a comparator reference voltage that is used to decide when to change from the 4x to the 3x multiplication factor.

The upconverter multiplier factor step size can be either ½ the battery voltage or one times the battery voltage in the following sequence: ½x, 1x, 1½x, 2x, 2½x, 3x, and 4x. When the step size should be ½ the battery voltage, a different reference voltage is applied to the comparator. This reference voltage is developed utilizing capacitance values for the capacitors, which are chosen in definite ratios to each other. One capacitor is initially connected in parallel with the battery while the other is shorted. Then during the sampling time the two capacitors are connected in parallel and a resultant voltage is developed. For example, for two capacitor which have a parallel capacitance total of 10 units, the first capacitor has a capacitance of 7 units and the second capacitor has a capacitance of 3 units. Thus for the first capacitor ratio of 7:10 and the second capacitor ratio of 3:10, the resultant voltage developed is 0.7 VBAT.

Another aspect of this invention uses a cross-coupled current mirror (Figure 3b, 3001, 3002) configuration to generate the threshold voltage, Vchargeth. A current mirror is used to generate a known, low value current (3005) that is run through two FETs (3003, 3004) operating in a sub-threshold condition. When operating in a sub-threshold condition, the drain current of an FET is exponentially related to the gate-to-source voltage, Vgs, such that for each approximately 100 m V of change in Vgs, the drain current will change by a factor of 10. If the size of two FETS (3003,3004) (which have their gates tied together and which are forced to have the same drain current by said current mirror) are chosen of values which are in the ratio of 10:1, then the FET that is 10 times larger will have a current density which is lower by a factor of 10. This results in Vgs of the larger FET being 100 m V different from the smaller FET. This 100m V potential is used as a reference voltage, with respect to the up/down voltage, into the comparator monitoring the state of charge of the stimulation capacitor.

Another aspect of this present embodiment is to produce a sub-threshold reference voltage, Vlowth , in the range 0.1 V to 0.8 V, using a similar current mirror method, as above , but developing a set voltage above ground voltage. This sub-threshold current is used to determine when the compliance voltage during the sample time is too low, so that the upconverter will move to the next higher multiplication scale factor.

In order to carry out switching control, the converter is set to a particular scale factor; a value is loaded into a 3-bit up/down counter. The output of this counter goes into a logic block that decodes this setting and enables or disables appropriate switches necessary to effect this scale setting. The clock then dynamically controls the actual turning on and off of these switching capacitors ("State 0"), and, second, the switch settings that deposit the charge onto the output reservoir capacitor ("State 1"). A two-phase clock is used with a separation between the phases so that there is an off time between states 0 and 1. This off time ensures that transient switching paths will not drain any of the charge off the switching capacitors, between state changes.

Figure 4 depicts the up/down converter ideal switch model. The capacitors to be electronically arranged are shown: C1 (401), C2 (402), C3 (403) and the reservoir capacitor Cr (404). Figure 5 shows the states of the up/down-converter with respect to the initial and final states of the capacitors, to operate the up/down-converter in the different multiplication factor modes. Resistors represent the switches. Figure 5a shows the switch and capacitor settings in a charging configuration (S0) and in a discharging configuration (S1) for a multiplying factor of ½ , that is a down-conversion mode. Capacitors C1 (401) and C2 (402) are used as well as switches (that are conducting) SW1 (501), SW6 (506), and SW8 (508) in the charging mode. In the discharging mode capacitors C1 (401) and C2 (402) are used together with switches SW1 (501),SW4 (504), SW7 (507) and SW12 (512).

Figure 5b has an analogous depiction for a multiplication factor of 1 utilizing only switches (that are conducting) SW3 (503), SW7

(507), SW8 (508), SW12 (512), SW13 (513), SW14 and (514). Figure 5c pictures an analogous situation for a multiplication factor of 1.5. Capacitors C1 (401) and C2 (402) are charged and discharged. Switches (that are conducting) SW1 (501), SW6 (506) and SW8 (508) are used in the charging state (S0); switches SW2 (502), SW5 (505), SW7 (507),SW12 (512) are utilized in the discharging mode. Figure 5d shows the multiplication factor 2 arrangements. Again capacitors C1 (401) and C2 (402) are charged and discharged. Charging makes use of switches (that are conducting) SW1 (501), SW3 (503), SW5 (505) and SW12 (512). Discharging utilizes SW2 (502), SW4 (504), SW7 (507), and SW8 (508).

Figure 5e presents the switch and capacitor combinations for the multiplication factor 2.5. Here the three capacitors are charged and discharged, C1 (401), C2 (402) and C3 (403). In the charging state, S1, the conducting switches are SW1 (501), SW6 (506), SW8 (508), SW9 (509) and SW13 (513). In the discharge state, S1, the conducting switches are SW2 (502), SW5 (505), SW10 (510), SW11 (511) and SW14 (514). Figure 5f shows the similar situation for the multiplication factor 3. C1 (401) and C2 (402) are the capacitors involved; conducting switches SW1 (501), SW3 (503) and SW4 (504) and SW8 (508) are on for the charging state; SW2 (502), SW6 (506) and SW12 (512) are on for the discharging state. Figure 5g is an analogous presentation for the multiplication factor 4. Here, the three capacitors C1 (401), C2 (402) and C3 (403) are charged and discharged. In the charging state, S0, the conducting switches are SW1 (501), SW3 (503), SW4 (504), SW8 (508) and SW13 (513). In the discharging state the conducting switches are SW2 (502), SW6 (506), SW11 (511), and SW14 (514).

In the automatic scale adjustment mode the output compliance voltage is sampled and compared to high and low thresholds. If this comparison indicates that the voltage is too low, the up/down counter will count up and a different combination of switches will be enabled to effect a higher multiplication factor. If the comparison indicates the voltage is too

high, the counter will count down and yet another combination of switches will be enabled that effect a lower multiplication factor.

The counter will only increment or decrement by one each time a sample of the compliance voltage is taken. When the counter reaches its minimum or maximum value, it will not further decrement or increment, respectively, even if the voltage sample indicates that a scale change is necessary.

While the invention herein disclosed has been described by means of specific embodiments and applications thereof, numerous modifications and variations could be made thereto by those skilled in the art without departing from the scope of the invention set forth in the claims.

CLAIMS

1. Circuit apparatus for supplying a current pulse to a load impedance, said apparatus comprising;

an output capacitor;

an output current control device for selectively discharging said output capacitor to produce an output current pulse through said load impedance; and

voltage control circuitry for producing a voltage signal to charge said output capacitor;

said voltage control circuitry including:

a battery supplying an output voltage VBAT;

a voltage converter circuit for producing a voltage signal VUPC, where VUPC is related to VBAT by an adjustable multiplication factor; and

means for adjusting said multiplication factor in response to a voltage VCOMPL representative of the voltage across said output capacitor.

2. The circuit apparatus of claim 1 including an output controller for defining the duration of said output current pulse.

3. The circuit apparatus of claim 2 wherein said output controller generates a sample clock proximate to the end of said output current pulse; and wherein

said means for adjusting said multiplication factor is responsive to said voltage VCOMPL measured at a time related to said sample clock.

4. The circuit apparatus of claim 2 wherein said output controller is programmable to define the duration and/or frequency of said output current pulse.

5. The circuit apparatus of claim 1 including a comparator for comparing said voltage values VUPC and VCOMPL; and

a clock controller responsive to said comparator for determining the rate of adjustment of said multiplication factor.

6. The circuit apparatus of claim 1 further including a recharge current control device responsive to said voltage signal VUPC for supplying a current to charge said output capacitor.

7. The circuit apparatus of claim 6 further including a programmed controller for controlling said recharge current control device.

8. The circuit apparatus of claim 1 wherein said battery is rechargeable.

9. An automatic up/down-converter comprising an upconverter circuit wherein the battery multiplication factor adjusts according to the amount of excess compliance voltage left at the end of a stimulation pulse.

10. The automatic up/down-converter as in claim 9 further comprising an adjustable battery voltage multiplication factor; said multiplication factor is increased when the excess compliance voltage is below a certain threshold voltage.

11. The automatic up/down-converter as in claim 9 further comprising an adjustable battery voltage multiplication factor; said multiplication factor is decreased when the excess compliance voltage is above a certain threshold voltage.

12. The automatic up/down converter as in claim 9 further comprising an automatic adjustable voltage converter clock rate wherein said clock rate is continuously adjustable.

13. A method for an automatic up/down converter comprising the step of adjusting an up/down-converter multiplication factor for the battery circuit according to the amount of compliance voltage left at the end of a stimulation pulse.

14. The method as in claim 13 further comprising the step of increasing said multiplication factor when the compliance voltage is below a certain threshold voltage.

15. The method as in claim 13 further comprising the step of decreasing said multiplication factor when the compliance voltage is a above a certain threshold voltage.

16. The method as in claim 13 further comprising the step of adjusting a voltage converter clock rate.

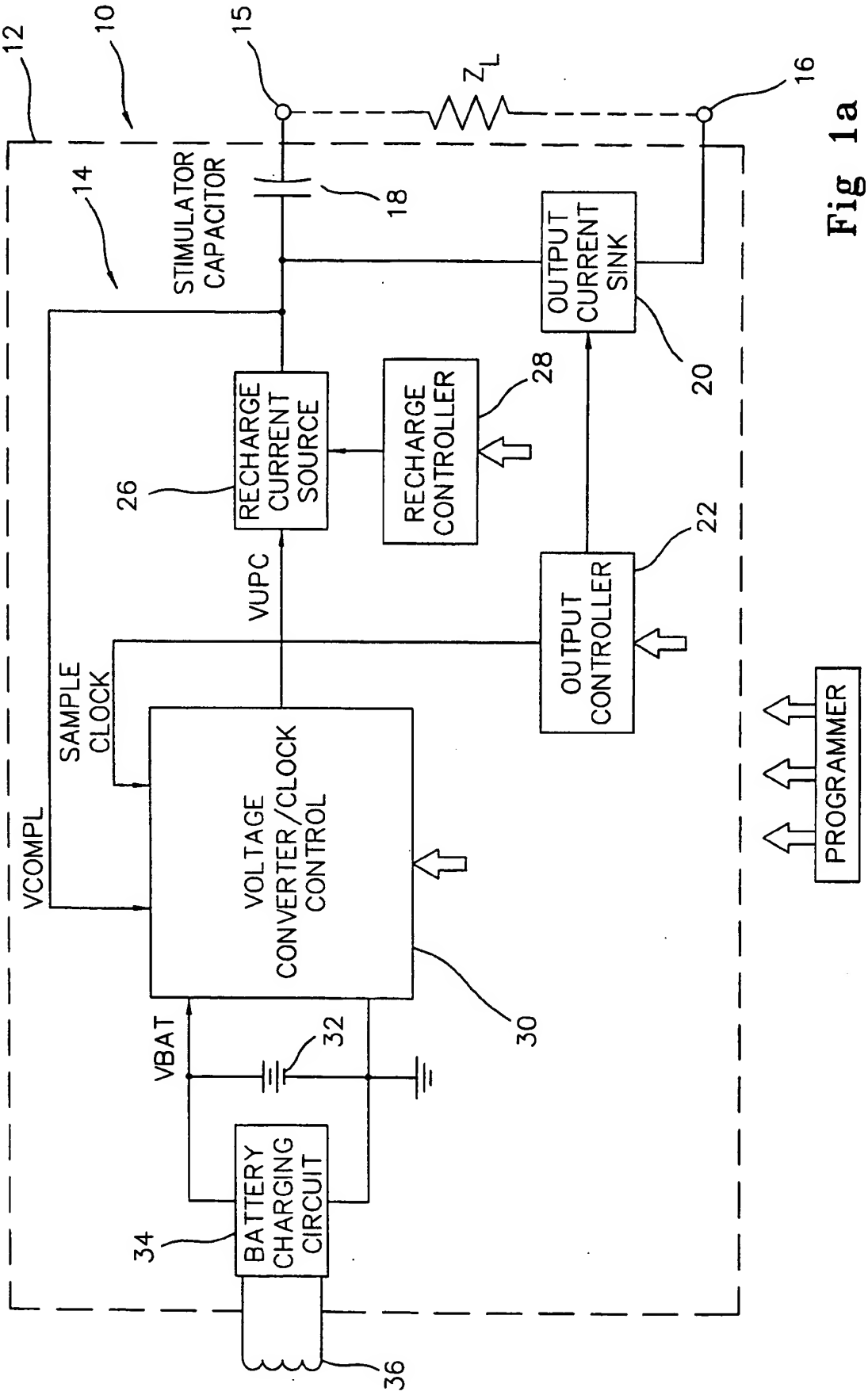

12
10
15
Z_L
16
14
STIMULATOR CAPACITOR
18
OUTPUT CURRENT SINK
20
28
RECHARGE CONTROLLER
26
RECHARGE CURRENT SOURCE
22
VUPC
OUTPUT CONTROLLER
SAMPLE CLOCK
PROGRAMMER
VCOMPL
VOLTAGE CONVERTER/CLOCK CONTROL
30
VBAT
32
34
BATTERY CHARGING CIRCUIT
36

Fig 1a

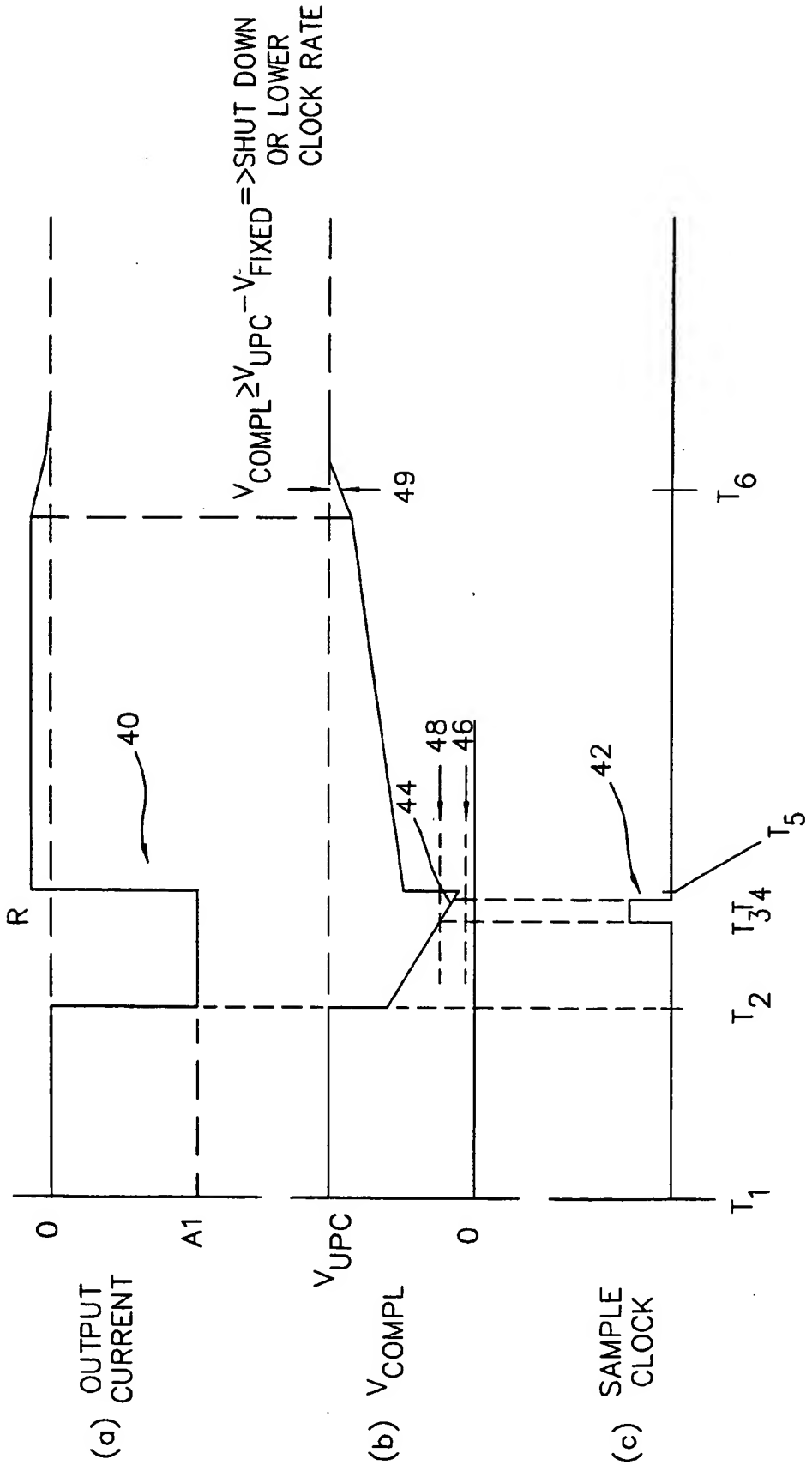

(a) OUTPUT CURRENT
0
A1
R
40
(b) V_{COMPL}
V_{UPC}
0
$V_{COMPL} \geq V_{UPC} - V_{FIXED}$ =>SHUT DOWN OR LOWER CLOCK RATE
49
44
48
46
(c) SAMPLE CLOCK
42
T_1
T_2
T_3
T_4
T_5
T_6

Fig 1b

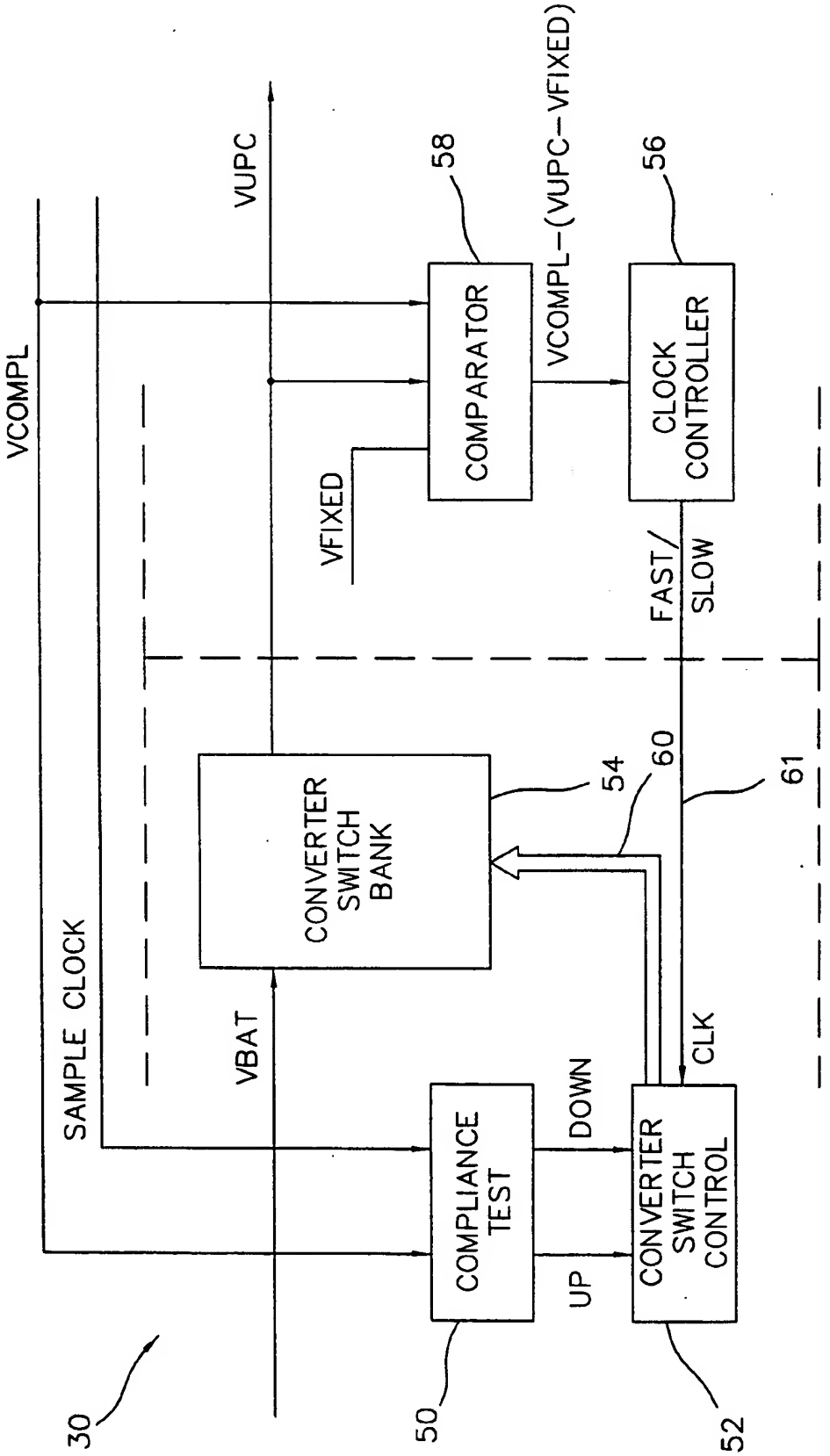

VCOMPL
VUPC
58
56
VCOMPL–(VUPC–VFIXED)
COMPARATOR
CLOCK CONTROLLER
VFIXED
FAST/
SLOW
CONVERTER SWITCH BANK
54
60
61
SAMPLE CLOCK
VBAT
CLK
DOWN
COMPLIANCE TEST
CONVERTER SWITCH CONTROL
UP
30
50
52

Fig 1c

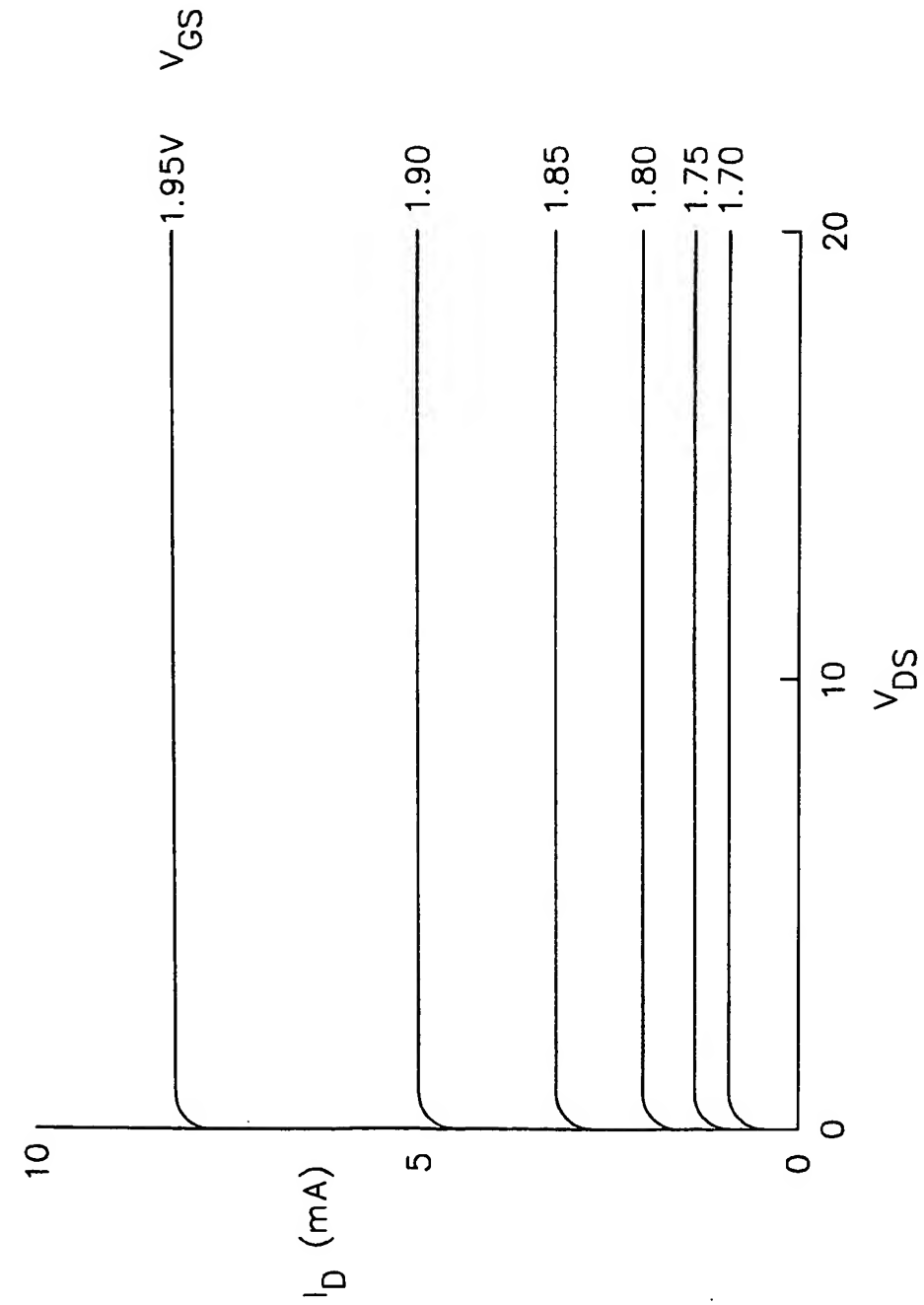


Fig. 1d

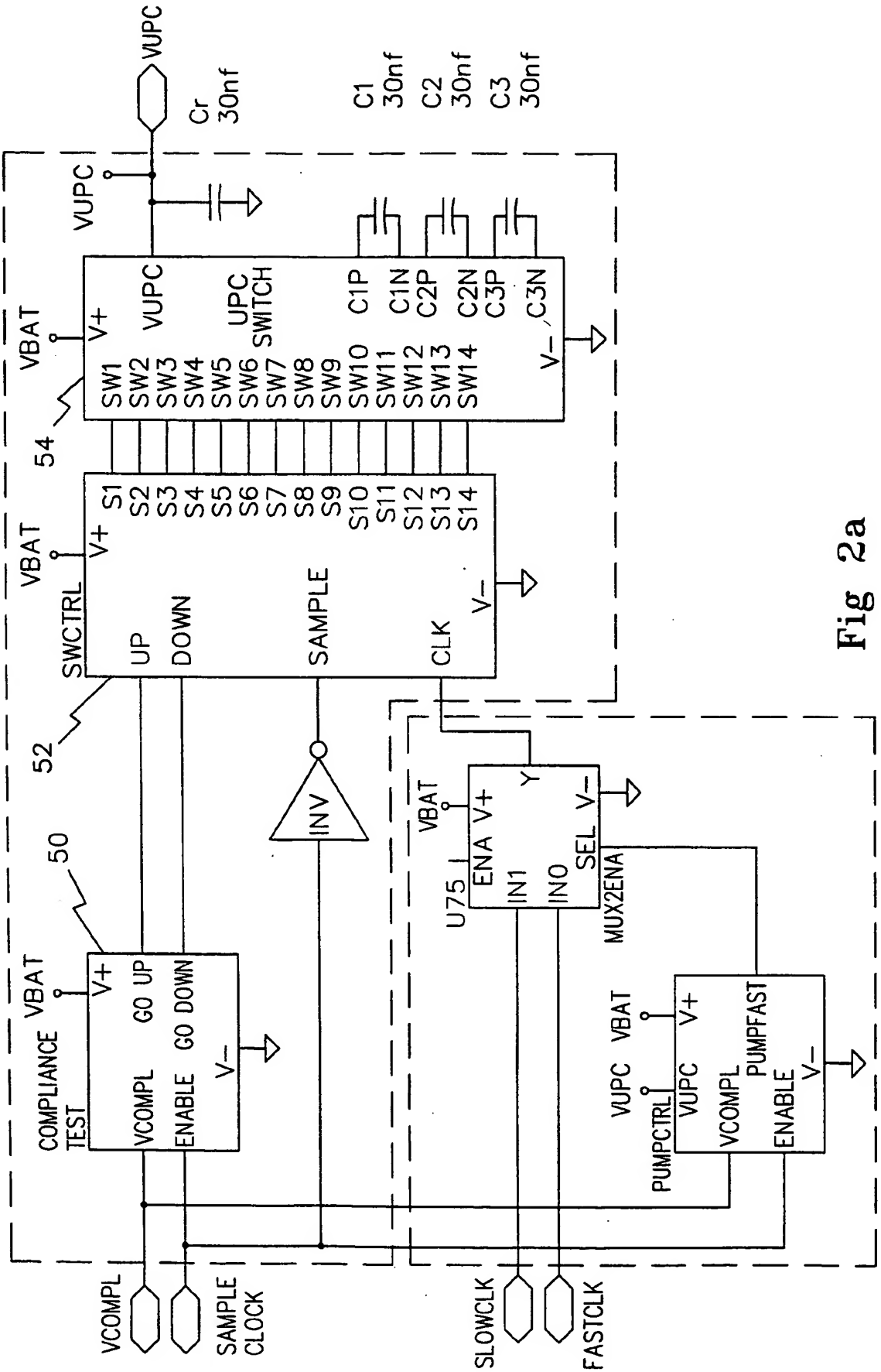

VUPC
Cr
30nf
C1
30nf
C2
30nf
C3
30nf
VUPC
VBAT
V+
VUPC
UPC SWITCH
C1P
C1N
C2P
C2N
C3P
C3N
V-
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
SW10
SW11
SW12
SW13
SW14
54
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
VBAT
V+
SWCTRL
UP
DOWN
SAMPLE
CLK
V-
52
INV
50
VBAT
V+
GO UP
GO DOWN
COMPLIANCE TEST
VCOMPL
ENABLE
V-
U75
VBAT
ENA
V+
Y
V-
IN1
IN0
SEL
MUX2ENA
VUPC
VBAT
V+
PUMPCTRL
VUPC
VCOMPL
PUMPFAST
ENABLE
V-
VCOMPL
SAMPLE CLOCK
SLOWCLK
FASTCLK

Fig 2a

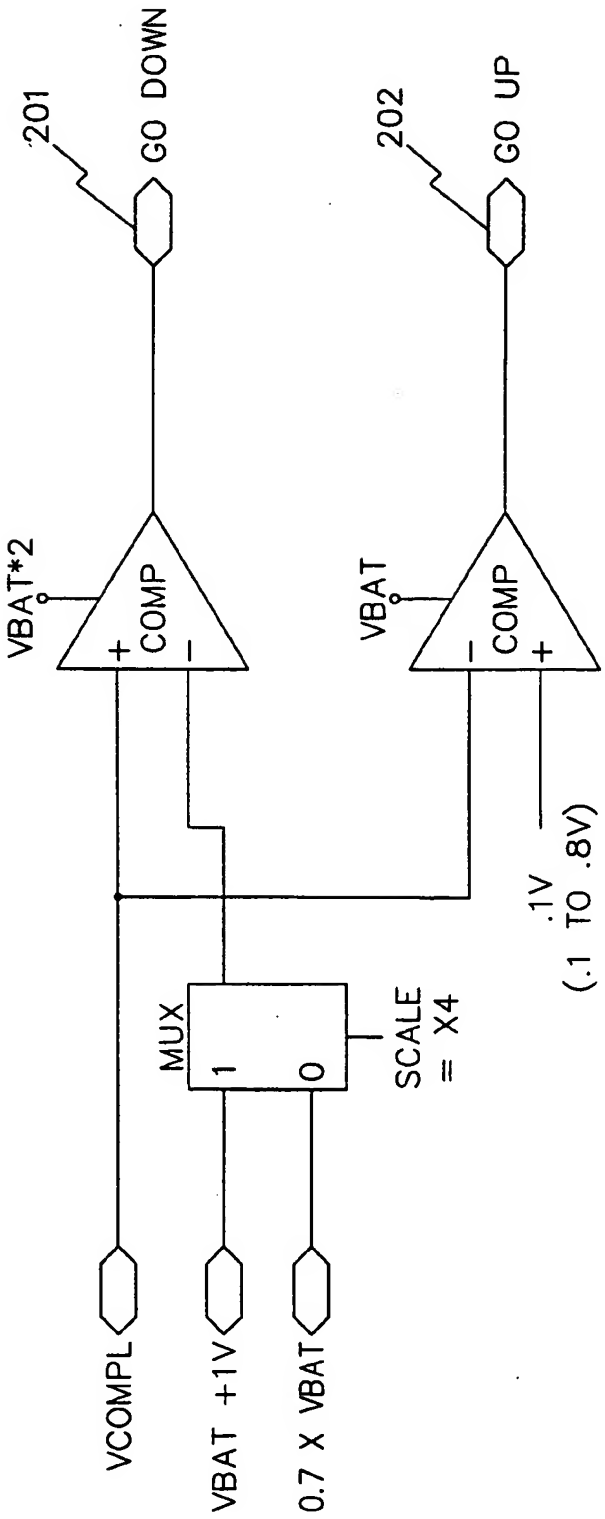

201
GO DOWN
202
GO UP
VBAT*2
COMP
VBAT
COMP
.1V
(.1 TO .8V)
MUX
1
0
SCALE
= X4
VCOMPL
VBAT +1V
0.7 X VBAT

Fig 2b

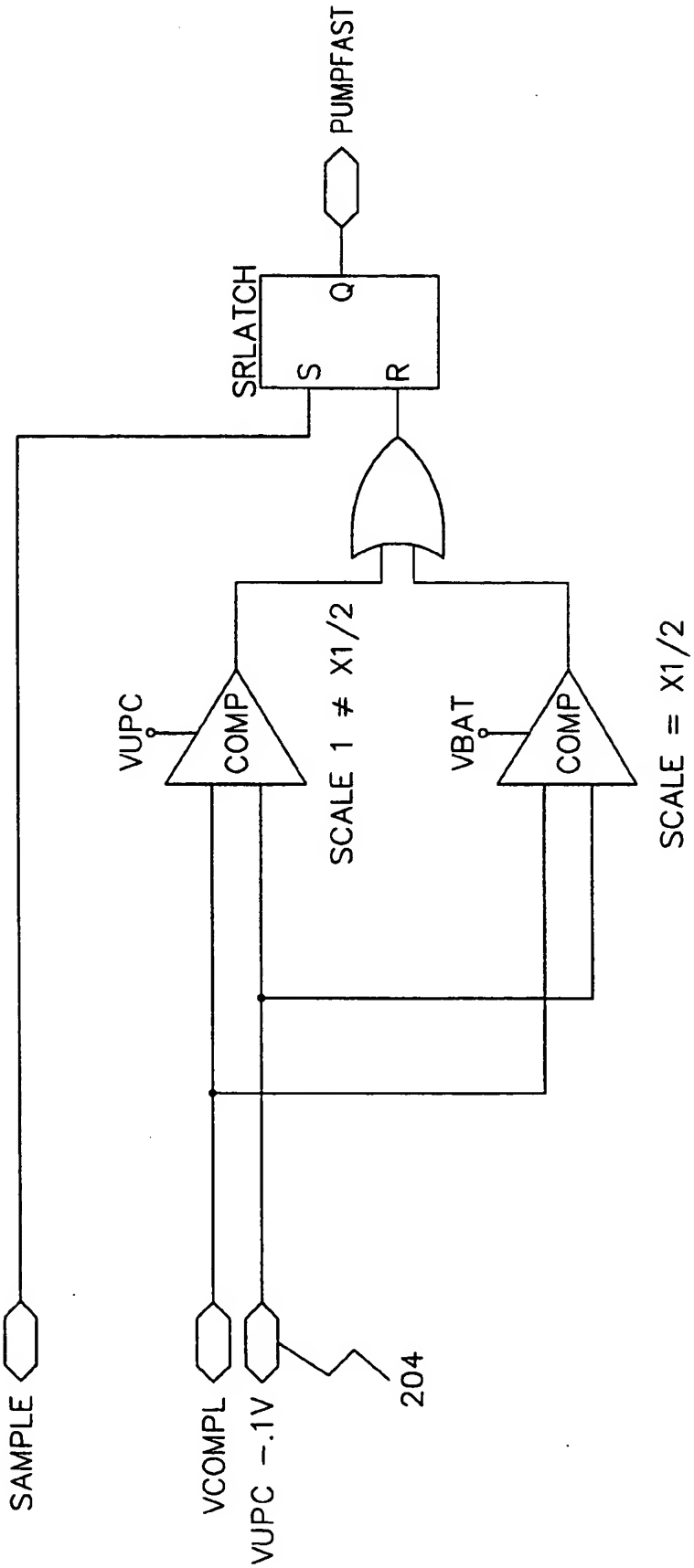

PUMPFAST
SRLATCH
Q
S
R
VUPC
COMP
SCALE 1 ≠ X1/2
VBAT
COMP
SCALE = X1/2
SAMPLE
VCOMPL
VUPC −.1V
204

Fig 2c

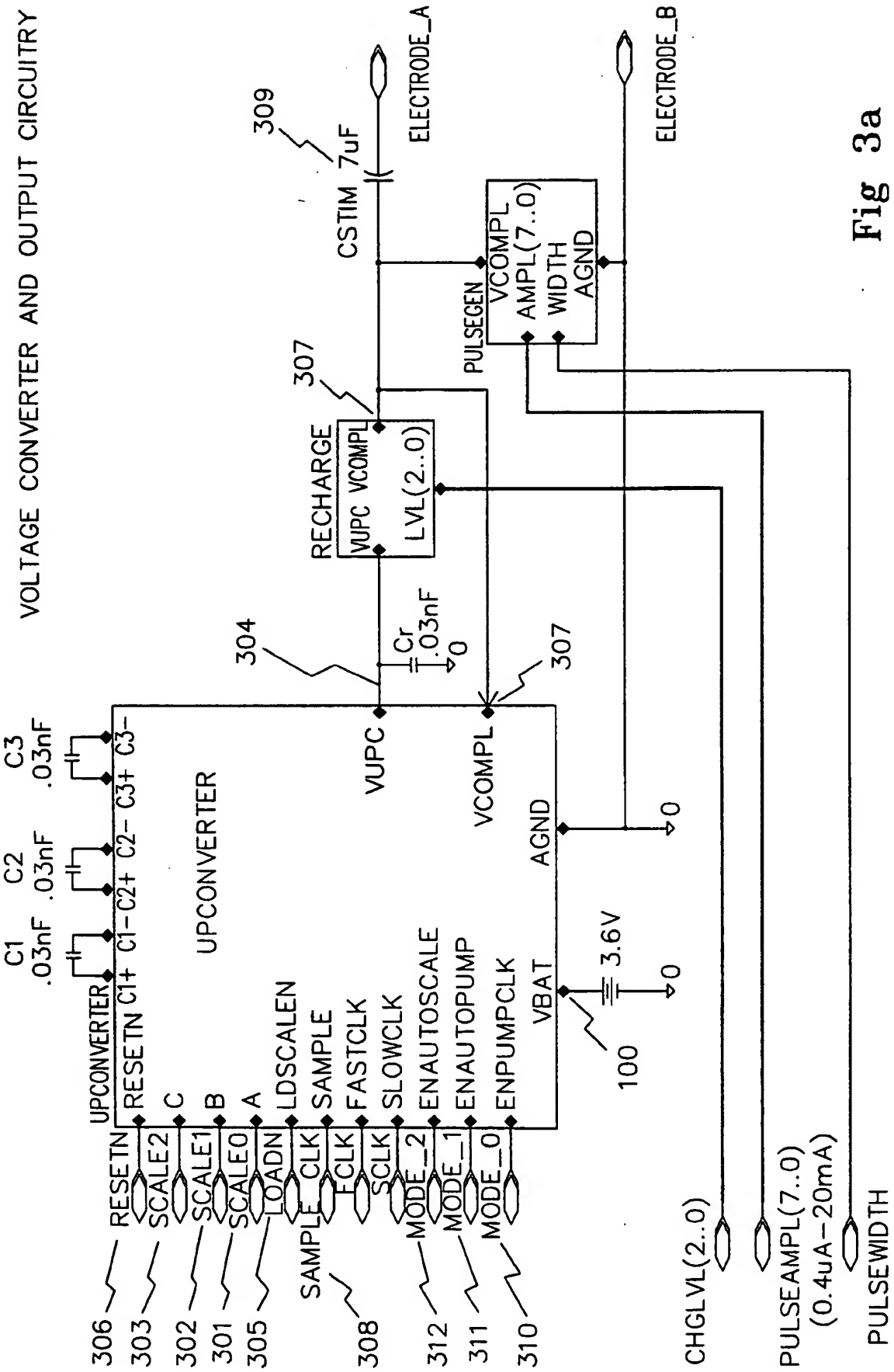

VOLTAGE CONVERTER AND OUTPUT CIRCUITRY
UPCONVERTER
RESETN
C1+
C1-
C2+
C2-
C3+
C3-
C
B
A
LDSCALEN
SAMPLE
FASTCLK
SLOWCLK
ENAUTOSCALE
ENAUTOPUMP
ENPUMPCLK
VBAT
AGND
VUPC
VCOMPL
C1 .03nF
C2 .03nF
C3 .03nF
Cr .03nF
3.6V
100
0
304
307
309
RECHARGE
VUPC VCOMPL
LVL(2..0)
PULSEGEN
VCOMPL
AMPL(7..0)
WIDTH
AGND
CSTIM 7uF
ELECTRODE_A
ELECTRODE_B
RESETN
SCALE2
SCALE1
SCALE0
LOADN
SAMPLE_CLK
FCLK
SCLK
MODE_2
MODE_1
MODE_0
306
303
302
301
305
308
312
311
310
CHGLVL(2..0)
PULSEAMPL(7..0)
(0.4uA–20mA)
PULSEWIDTH

Fig 3a

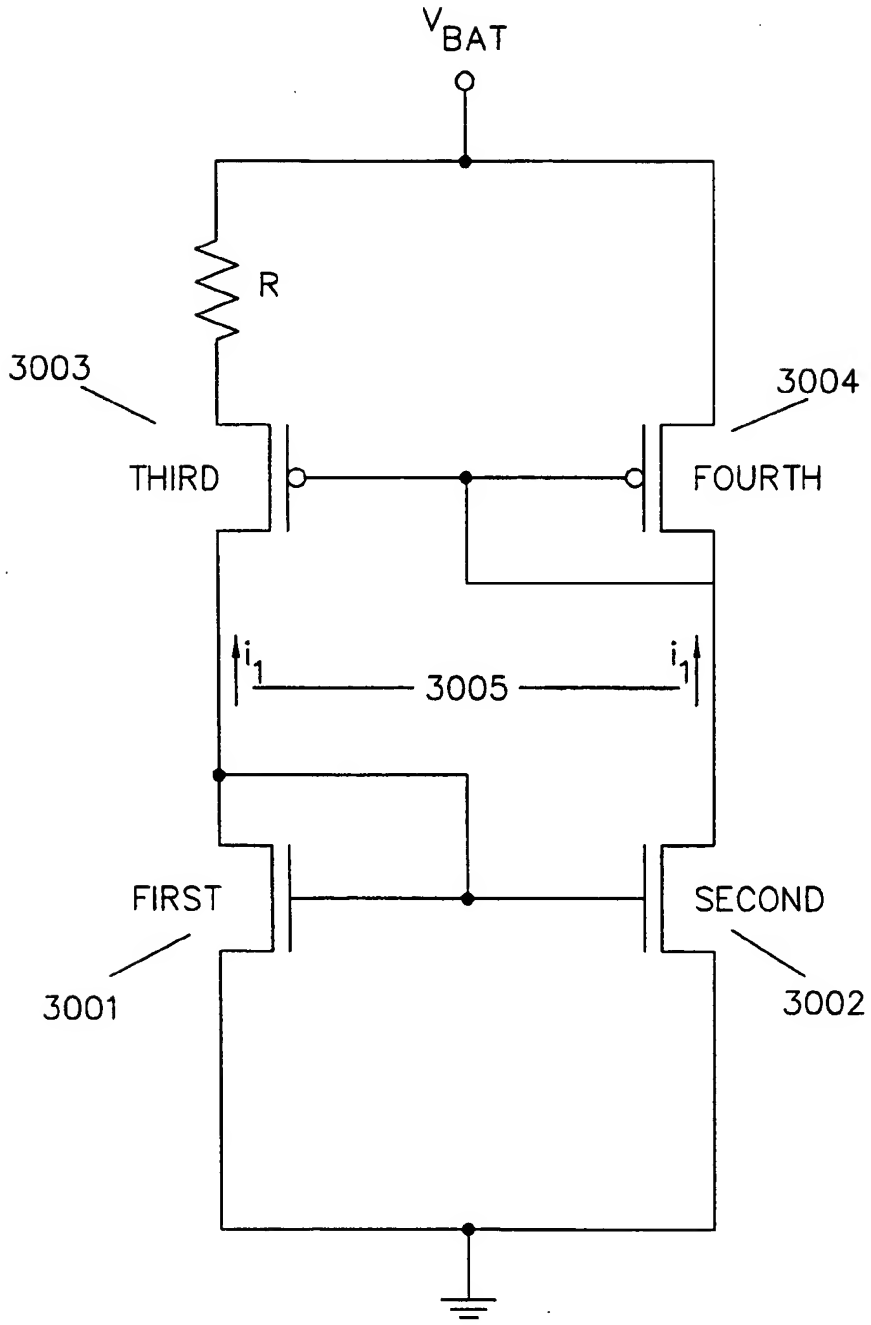

V BAT
R
3003
3004
THIRD
FOURTH
i1
3005
i1
FIRST
SECOND
3001
3002

Fig 3b

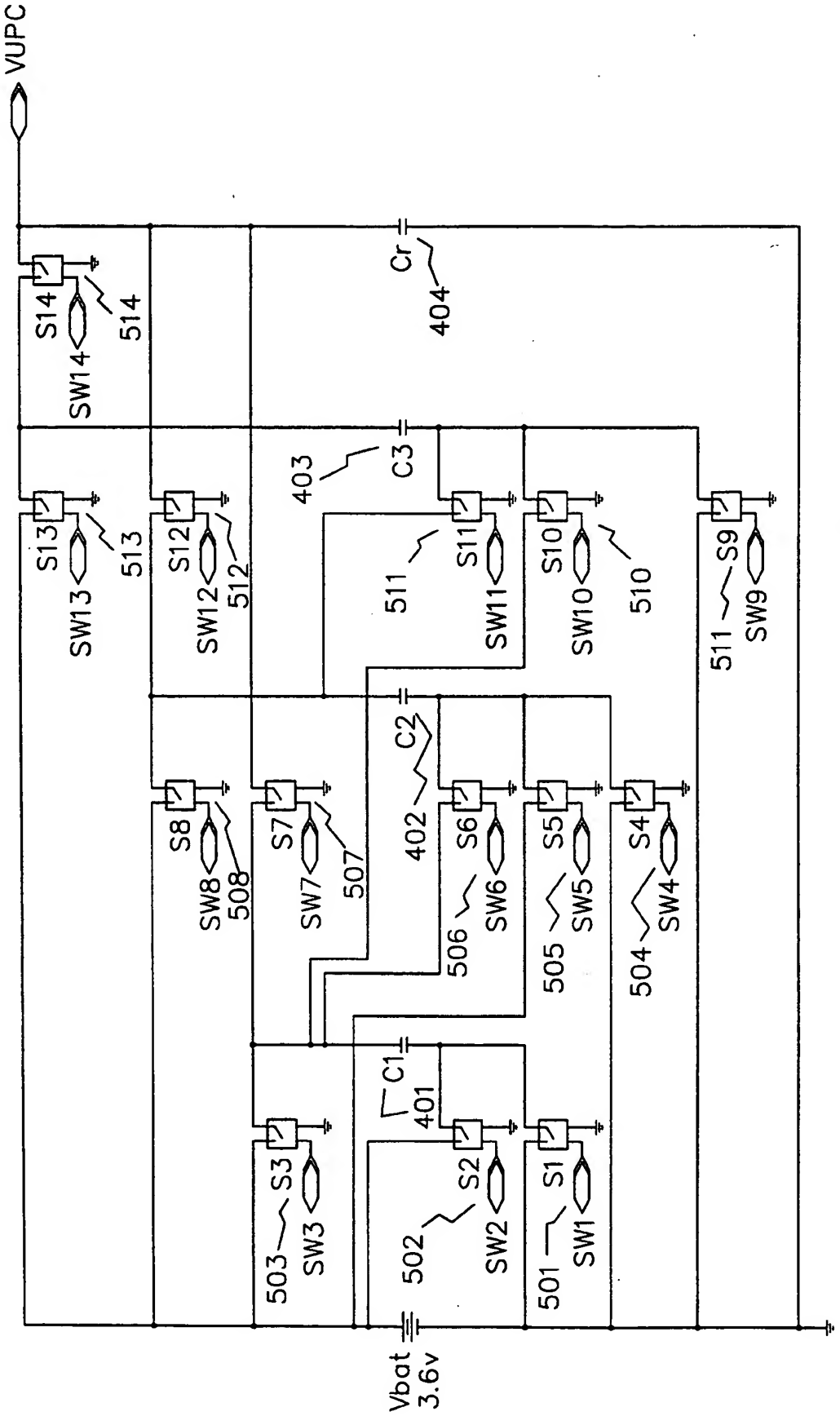

VUPC
S14
SW14
514
Cr
404
403
C3
S13
SW13
513
S12
SW12
512
511
S11
SW11
S10
SW10
510
511
S9
SW9
C2
402
S8
SW8
508
S7
SW7
507
S6
SW6
506
S5
SW5
505
S4
SW4
504
C1
401
S3
SW3
503
S2
SW2
502
S1
SW1
501
Vbat
3.6v

Fig 4

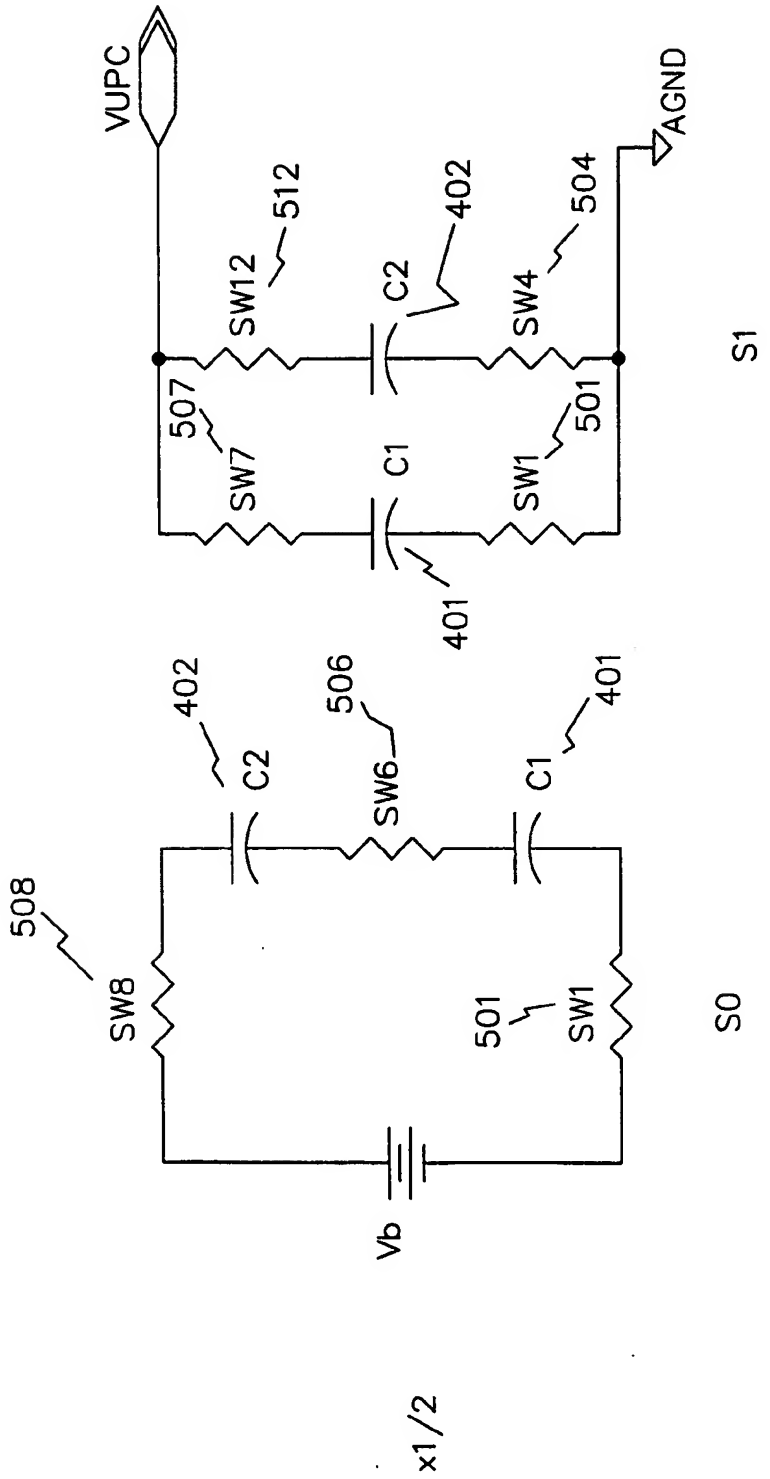

VUPC
AGND
512
SW12
402
C2
504
SW4
507
SW7
C1
501
SW1
401
S1
402
C2
506
SW6
401
C1
508
SW8
501
SW1
S0
Vb
x1/2

Fig 5a

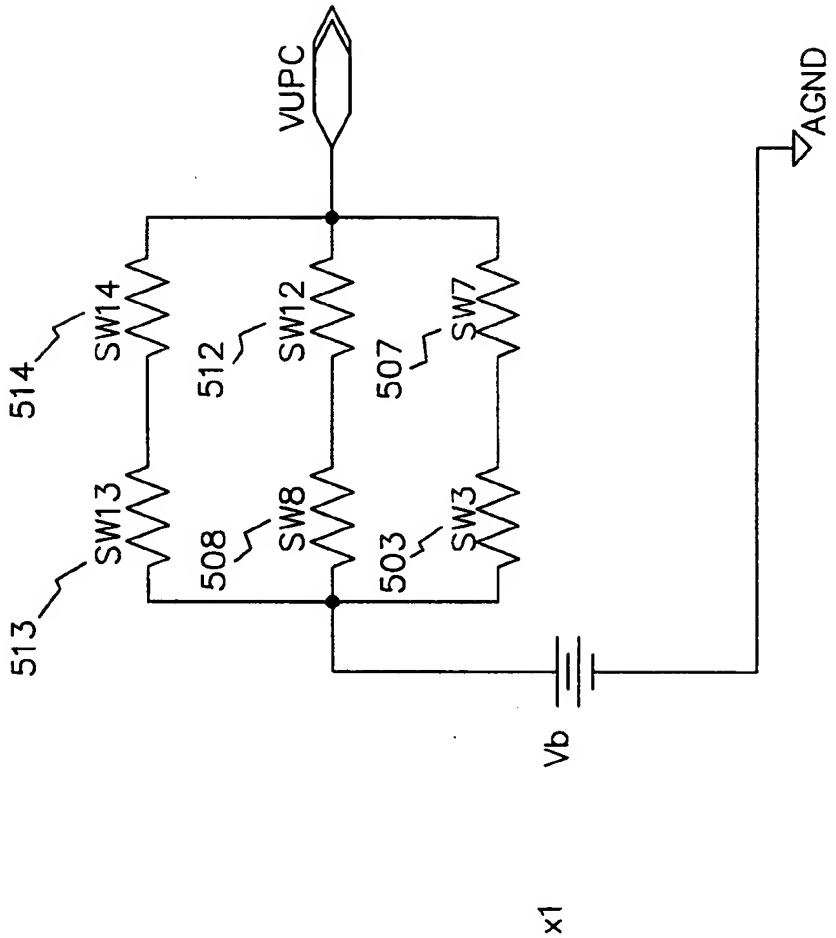

VUPC
AGND
514
SW14
512
SW12
507
SW7
513
SW13
508
SW8
503
SW3
Vb
x1
S0,S1

Fig 5b

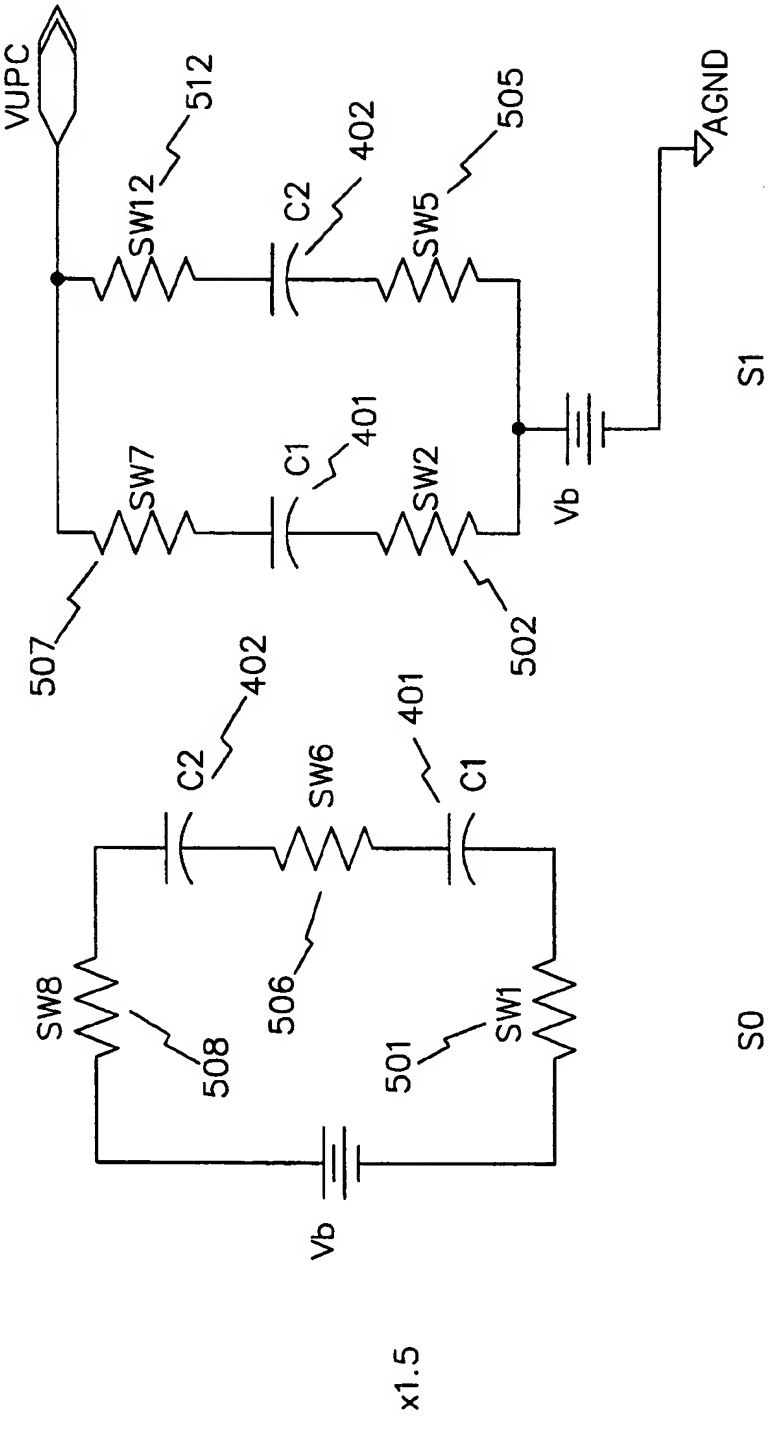

VUPC
512
SW12
C2
402
SW5
505
AGND
S1
SW7
C1
401
SW2
Vb
507
502
C2
402
SW6
401
C1
SW8
508
506
501
SW1
Vb
S0
x1.5

Fig 5c

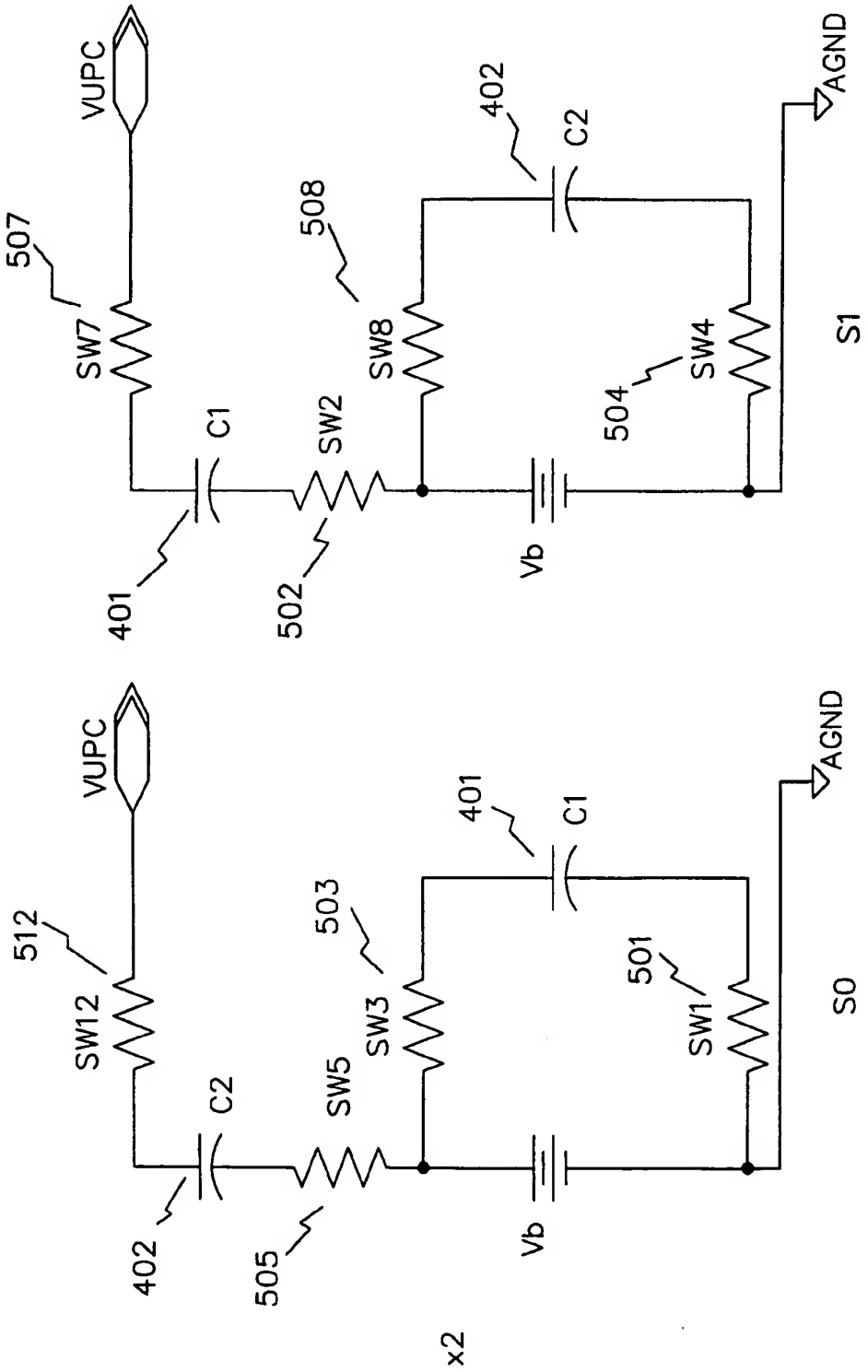

VUPC
507
SW7
C1
401
SW2
502
508
SW8
Vb
402
C2
504
SW4
AGND
S1
VUPC
512
SW12
C2
402
SW5
505
503
SW3
Vb
401
C1
501
SW1
AGND
S0
x2

Fig 5d

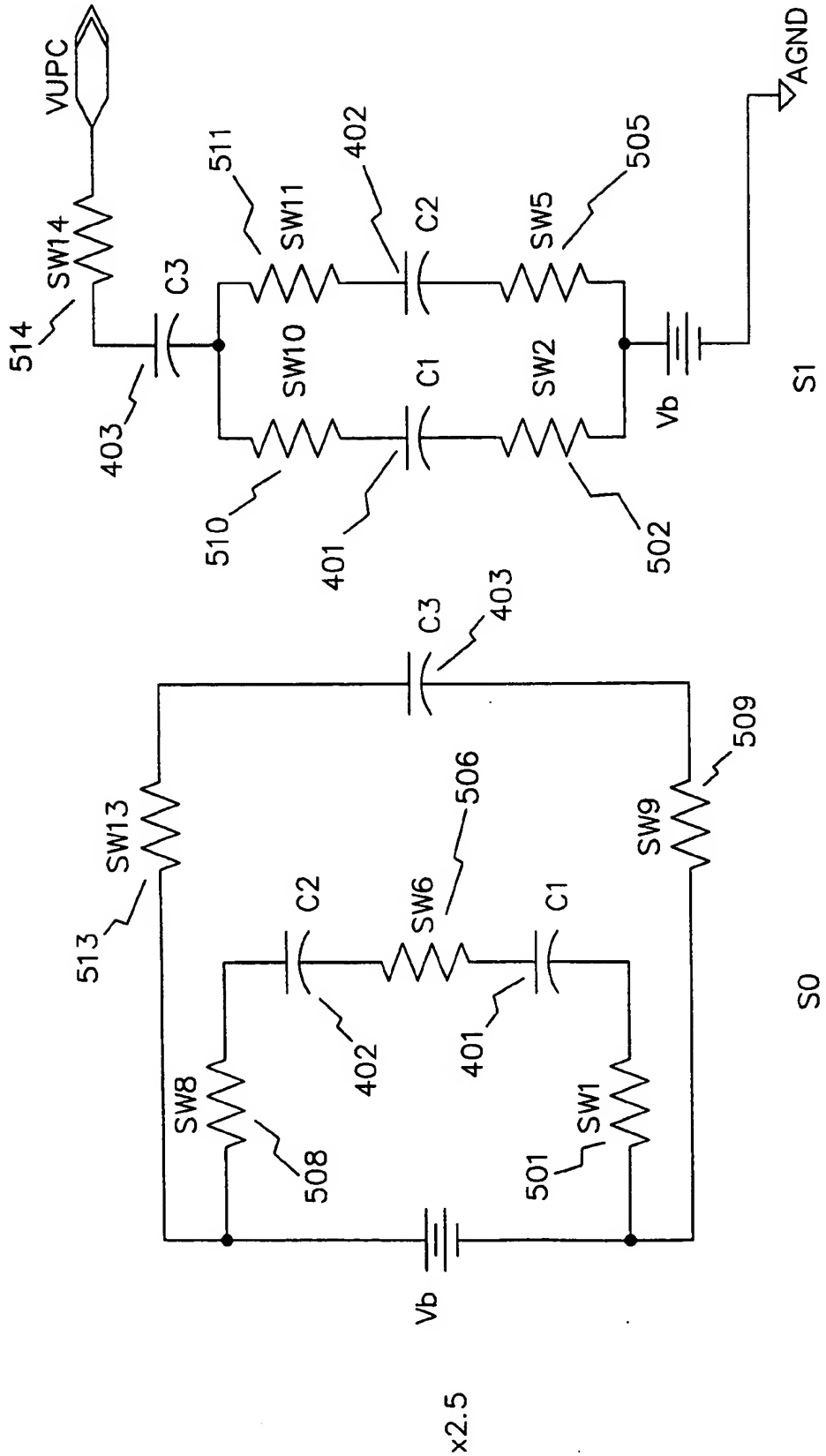

VUPC
SW14
514
C3
403
SW11
511
SW10
510
C2
402
C1
401
SW5
505
SW2
502
AGND
S1
Vb
C3
403
SW13
513
SW9
509
C2
SW6
506
C1
402
401
SW8
508
SW1
501
S0
Vb
x2.5

Fig 5e

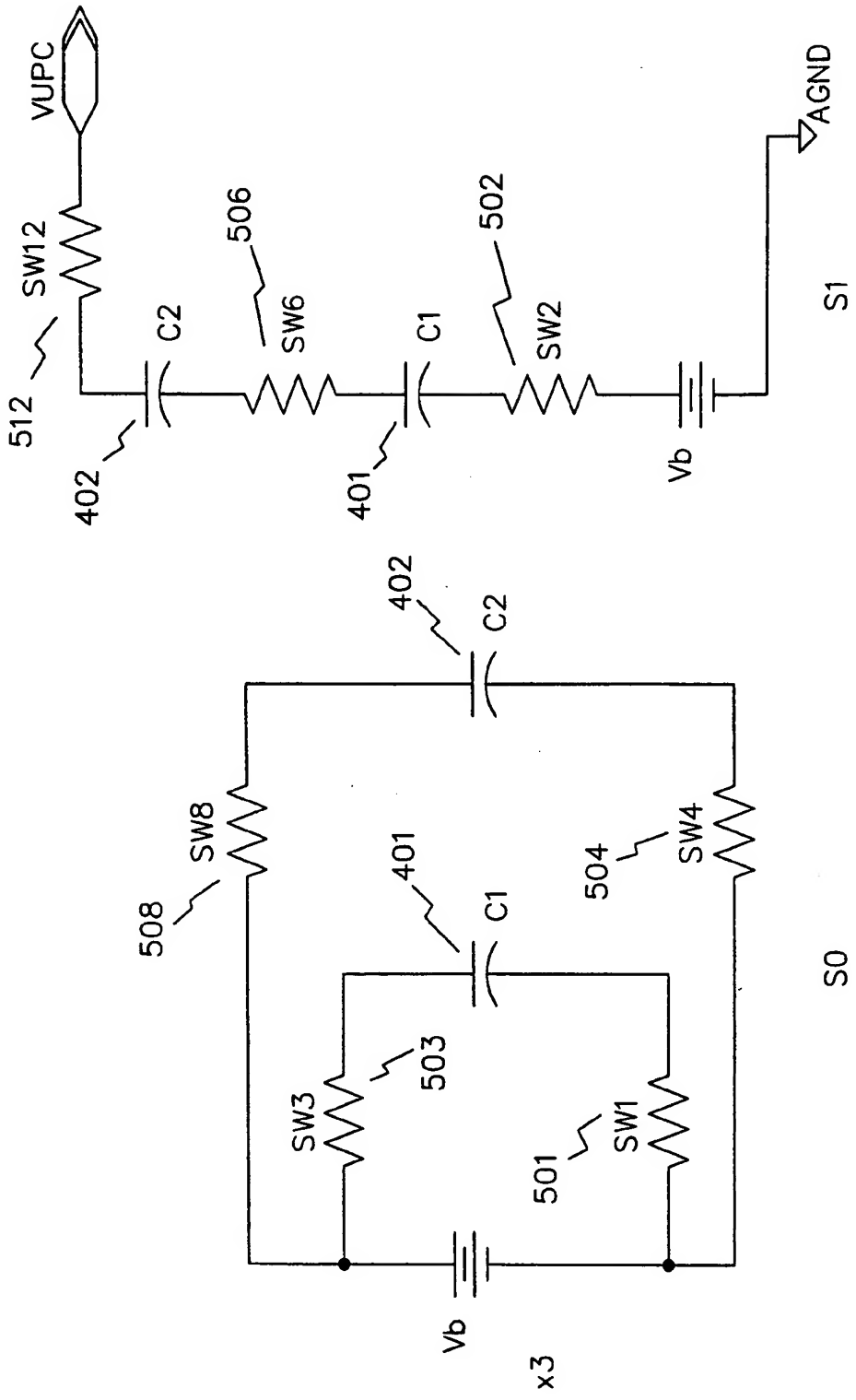

VUPC
SW12
512
C2
402
506
SW6
C1
401
502
SW2
Vb
AGND
S1
402
C2
SW8
508
401
C1
504
SW4
503
SW3
501
SW1
Vb
x3
S0

Fig 5f

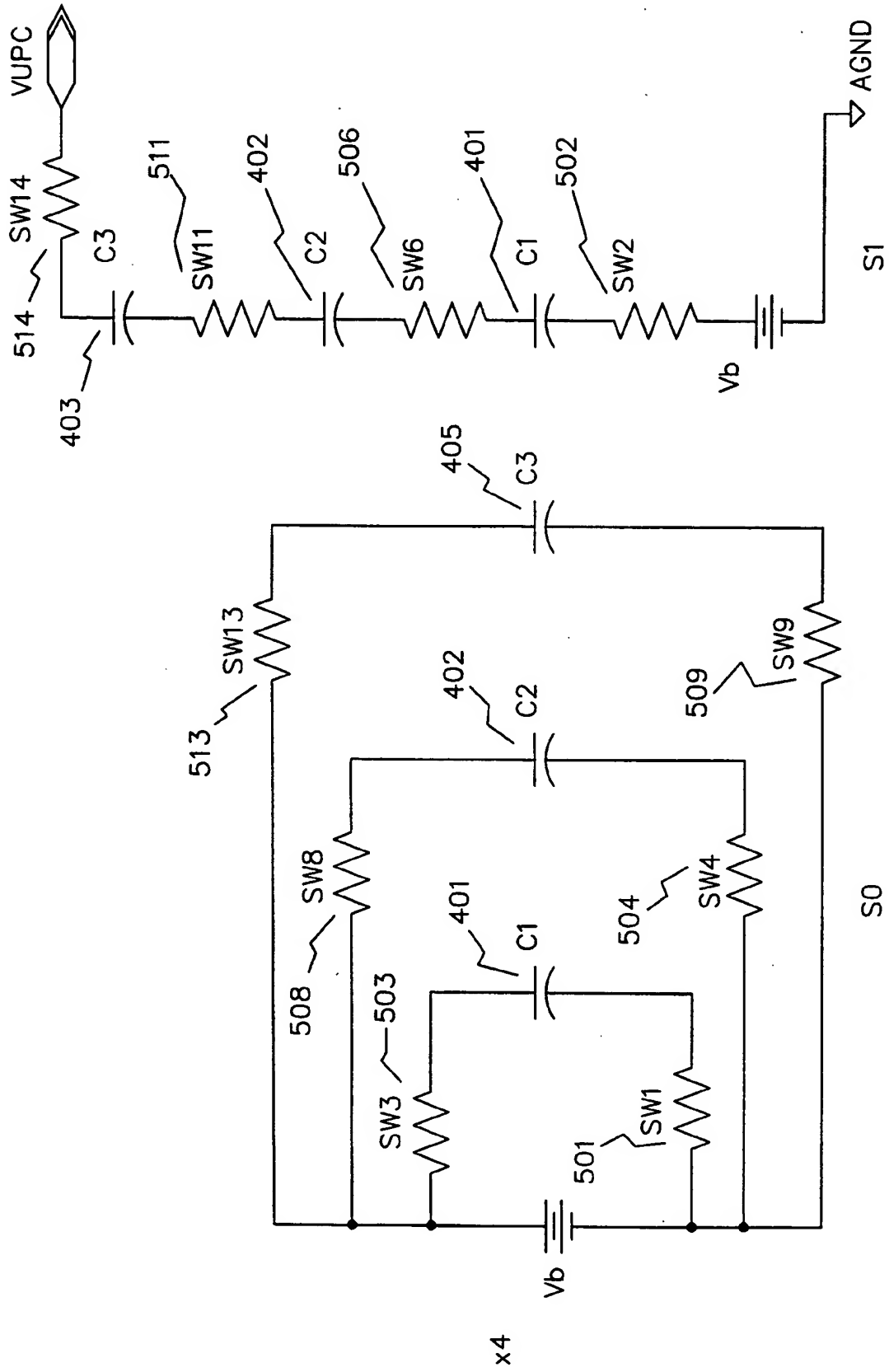

VUPC
SW14
514
C3
403
511
SW11
402
C2
506
SW6
401
C1
502
SW2
Vb
AGND
S1
405
C3
SW13
513
SW9
509
402
C2
SW8
508
401
C1
503
SW3
SW4
504
SW1
501
Vb
S0
x4

Fig 5g

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/20379

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H02J 7/00, 7/04, 7/16; H02M 7/00, 7/19, 7/25; A61N 1/18, 1/24, 1/32, 1/36, 1/38
US CL : 320/166, 160, 161, 162; 607/56, 61, 115; 363/59, 60, 61, 62
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 320/166, 160, 161, 162; 607/56, 61, 115

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
USPTO APS Derwent, JPOABS, EPOABS search terms: multplying, mulplier, factor, charge pump

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,418,751 A (KAISER) 23 May 1995 (23.05.1995), see entire disclosure.	1-16
X	US 5,424,934 A (TANUMA et al.) 13 June 1995 (13.06.1995), see entire document.	9-16
---		------
Y		1-8
Y	US 5,285,779 A (CAMERON et al.) 15 February 1994 (15.02.1994), figure 2.	1-8
A	US 5,702,424 A (LEGAY et al.) 30 December 1997 (30.12.1997), figure 1.	1-8

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search
19 September 2000 (19.09.2000)

Date of mailing of the international search report
02 NOV 2000

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Form PCT/ISA/210 (second sheet) (July 1998)